Multichannel Analyzer 6240





AN LEGIG COMPANY



Operating Modes

PHA
The Pulse Height Analysis mode permits

rapid accumulation of spectra based on energy, time, or other parameters that can be represented by the peak amplitude of a pulse. The resulting spectra are histograms of the amplitude distribution of the input pulses. The range of the parameter being studied is determined by the preamplifier-amplifier system rather than by the MCA itself. Remote control operation with this mode is possible through rear panel connectors.

ADC Channel Resolution 8192 maximum.

Clock Rate 100 MHz.

Differential Nonlinearity ≤±1.0% over the top 99% of full scale.

Integral Nonlinearity ≤±0.05% over the top 99% of full scale.

Temperature Instability ≤±0.01%/°C, 0 to 50°C.

Preset Count or Live Time Variable from 10 to 800,000 counts or seconds.

Dead Time Per Event $(3 + 0.01N + T_p)$ μ s, where N is the final channel address of the digitized pulse and T_p is the time for the pulse to peak.

TEST

The Test mode, for convenient memory check, provides automatic addition or subtraction of counts to each channel of a displayed spectrum at the rate of the display sweep. This convenient feature allows a visual check of the memory circuits.

MCS OR MCSR

The Multichannel Scaling and Multichannel Scaling Repeated modes permit the 6240 to function as a series of sequentially assigned counters to count input pulses through controlled intervals of dwell time. The MCS mode consists of a single scan of all memory channels, followed by an automatic stop, whereas the MCSR mode permits a recycling of the scan after each pass, with the accumulation stopped manually or externally.

Dwell Time Per Channel Selectable from 10 to $800,000 \mu s$.

Storage of Sweeps Number of sweeps made in MCSR stored in channel 0.

Dead Time Between Channels <3 μs.

Count Rates 5 MHz acceptable.

Channel Advance Logic Signals Available on rear panel.

Channel Advance Control Connector on rear panel for remote operation.

Signal Processing

SCA

The single channel analyzer in the 6240 performs a preliminary analog amplitude discrimination on each input pulse to ensure that the lower and upper amplitude limits have been satisfied before the actual digitizing of the amplitude is begun. A 10-turn Lower Level potentiometer, a 10-turn Upper Level potentiometer, and an Adjust/Operate switch set the operating range. The Lower Level discriminator range is 0 to 10 V, and the Upper Level range is 0.5 to 10.5 V. The Adjust/Operate switch selects a sliding pulser to simplify setting of SCA limits

by visual inspection of the cathode-ray tube without affecting the stored data. A rear panel BNC connector provides a pulse for each ADC input pulse that meets the SCA limitations.

ADC

The analog-to-digital converter in the 6240 converts the amplitude of an analog pulse into a digital number that is proportional to the amplitude of the input pulse. The 100-MHz ADC has a maximum resolution of 8192 channels, with the conversion gain adjustable from 8192 to 256 channels in binary increments. The

dead time per pulse reduces proportionately as the conversion gain is decreased from 8192 to 1024 channels; the percent of dead time is monitored with a front panel meter. The digital offset is variable from 0 to 7936 channels in steps of 256 channels. A Zero Adj potentiometer allows the dc baseline to be adjusted over the range +0.25 V to -0.25 V. Since the dc baseline is prealigned for each Address Full Scale setting, it is not necessary to adjust the zero level each time the conversion gain is changed. Both ac- and dc-coupled ADC Input connectors on the front panel are bridged to connectors on the rear panel to provide alternate locations; a separate MCS Input connector is available on the rear panel. ADC input signals with amplitudes of 0 to 10 V and rise times of 0.5 to 30 us are acceptable. The Gate Input, which can be operated in anticoincidence, off, or coincidence modes, requires input signals that are TTL-compatible. These signals should have amplitudes greater than 3 V for true logic and less than 1.5 V for false logic. The minimum effective gating pulse width is approximately 0.5 µs. All input impedances are approximately 2000Ω .



Memory and Preset Controls





The 6240 MCA has a fail-safe ferrite core memory that retains all data in the event of a power failure. The memory is in a 25-bit parallel configuration, with 24 bits used to store BCD data and 1 bit reserved as a region of interest (ROI) flag. The count capacity is 10^6-1 counts per channel and the memory cycle time is less than 3 μ s. The MCA with 1024 channels of memory (6240-01) can be upgraded later to 4096 channels of memory (6240-04).

Subgroups of full, halves, or quarters can be selected by a front panel Storage Region switch or by external routing; memory halves or quarters can be overlapped as they are displayed on the CRT. Data can be transferred from memory subgroup 1 to any other subgroup by pressing the Xfer button. The memory can be erased by pressing the Erase push buttons or by using an external positive logic signal. Pressing the left memory Erase push button erases only channel 0;

pressing both push buttons erases all channels. A Storage Mode switch in the Memory section allows the data to be added, subtracted, or unaltered (Off).

The Test Mode used in conjunction with the Sub(tract) Storage Mode allows the background to be stripped from a peak; then, with an optional Integrator (6240-07), the net counts above background can easily be determined.

Preset controls allow restrictions, in the PHA mode, of live time (in seconds) or counts (in a channel or region of interest) over the range 10 to 10^5 , with a multiplier selection of 1, 2, 4, or 8. Preset time status is stored in channel 0; preset count status is stored in channel 1. In the MCS or MCSR mode, clock dwell time per channel is selectable from 10 to 800,000 μ s/channel, and the number of sweeps is stored in channel 0.

Display

The memory contents are displayed on a built-in 8- by 10-cm cathode-ray tube at a rate of 100 kHz. The display mode can be either live or static.

Any number of ROIs (regions of interest), not necessarily contiguous, can be defined and will appear as intensified regions on the CRT. These ROIs can be set, left unchanged, or cleared by using the scanning Marker switch. An optional Character Generator (6240-06) permits the display on the CRT of (1) the characters "Ch" followed by the 4-digit

number corresponding to the scanning marker location and (2) the 6-digit contents number of the marker channel preceded by the characters "Co". An optional Integrator (6240-07), in conjunction with the Character Generator, provides for the display of the 8-digit number that is the integral of the ROI in which the marker is located. Preset time status, preset count status, or the number of sweeps made while the 6240 is in the MCSR mode can all be displayed on the CRT.

The full-scale linear ranges are 100, 500, 1K, 5K, 10K, 50K, 100K, 500K, and 1M counts. A 6-decade Logarithmic Display range is optional (6240-08). Both vertical and horizontal expansion controls are continuously adjustable, with the vertical expansion ranging from X1 to X5 and the horizontal expansion from X1 to X8. In the spectra Overlap mode the Vertical Expand control allows normalization of the spectra for direct comparison. A Full Scale Calibrate switch is included for calibration of the CRT display or an external x-y recorder.

The normal CRT controls for Focus, Vertical Position, Horizontal Position, Intensity, and scale illumination (Graticule) are provided.



Data Transfer

Analog outputs for an x-y recorder and NIM daisy-chain printing capability for ORTEC scalers and timers are standard features of the 6240. Optional output interfaces for a Teletype®, paper-tape perforator, and parallel printer are available. The Teletype interface transfers data in a serial-character, parallel-bit train in ASCII code. Front panel controls allow all outputs to be restricted to the contents and identification of only those

channels in the ROI or to only the integrals and identification of the ROI.

Another option is the PDP11 Computer Interface (6240-6551), which allows parallel transfer in and out of data in all channels (including live time in PHA. preset count status, or the number of MCS sweeps), ROI definition, and channel identification.

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Electrical and Mechanical

POWER REQUIRED

117 Vac, 50 to 60 Hz, or 230 Vac, 50 to 60 Hz; power dissipated, ~200 VA.

DIMENSIONS

8-3/4 in. (22 cm), high, 22 in. (56 cm) deep overall; front panel width compatible with 19-in. (48-cm) relay rack or cabinet.

WEIGHT

Shipping ~125 lb (~57 kg).

6240-01

MCA with 1024 channels of memory

6240-04

MCA with 4096 channels of memory

Data Assembler and Teletype Interface

6240-06

Character Generator; requires -05 option

Integrator; requires -05 option

Logarithmic Display

6240-6551

PDP11 Computer Interface

Cover for table top use (see photo on front cover)

Net ~54 lb (~25 kg).

Basic MCAs and Options

6240-05

6240-07

6240-08

Call your local ORTEC representative or our Oak Ridge office for information on output interfaces and devices and computerized systems.

Rear Panel Connectors

BNC CONNECTORS

The group of connectors for the ADC section includes AC In, DC In, Gate In, and SCA Out; except for SCA Out these connectors are bridged to corresponding front panel connectors.

The Controls connectors - Run In, CRT In, I/O In, and Memory Erase In - accept external signals to allow remote control of the associated functions

An MCS Channel Advance Input connector accepts external pulses (when the adjacent switch is set to the Ext position) that provide channel advance in MCS or MCSR modes. Other MCS connectors are Input, which accepts logic signals to be counted into an assigned channel during MCS or MCSR operation; Channel Adv Out, which furnishes a signal to indicate the intervals of dwell time and channel advance; and End of Sweep Out, which furnishes a signal to indicate the completion of each sweep through the memory.

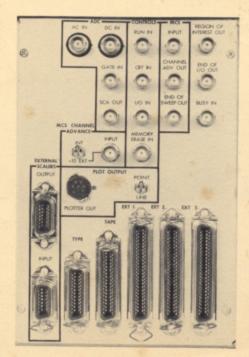
The Region of Interest Out connector furnishes a logic pulse to indicate that the channel selected during PHA has an ROI status; the End of I/O Out connector furnishes a logic pulse to indicate that a readout program has been completed; and the Busy In connector accepts external signals to correct for the dead time that occurs in the front-end electronics, as in a pulsed optical feedback system.

MULTIPIN CONNECTORS

A 7-pin Plotter Out connector is included that is compatible with the standard cable from a Hewlett Packard Model 7004B x-y plotter, or equal. A Point/Line toggle switch allows the plotter to be operated in the mode desired.

Two 14-pin Output/Input External Scalers connectors accommodate any external ORTEC printing modules (counters and timers) that may be included in the printing loop to an external serial-bycharacter printing accessory.

Other multipin connectors include Type, which accepts the standard cable from an ORTEC 222, a Teletype model 33 ASR page printer modified to accept parallel transfer of data; Tape, which is reserved for connection of digital magnetic tape or paper tape devices; Ext 1, which has pins for signals controlling mode selection, subgroup routing by halves or quadrants, and miscellaneous programming control lines; and Ext 2 and 3, which are reserved for computer and parallel interface applications.



For more information on ORTEC products or their applications, contact your local ORTEC Europe: ORTEC GmbH, P. O. Box 860646, Herkomerplatz 2, 8000 Munich 86, West Germany: Telephone (089) 98-71-73; Telex United Kingdom: ORTEC Limited, Dallow Road, Luton, Bedfordshire, England; Tele-phone LUton (0582) 27557/8/9; Telex 82477 Other: ORTEC Incorporated, 100 Midland Road, Oak Ridge, Tennessee 37830; Telephone (615) 482-4411; TWX 810-572-1078; Telex 055-7450 INCORPORATED ₩ EGEG